# Operation and Installation Manual

Niagara NT 944

Pentium MMX, 75-233MHz System Board
supporting AMD K6

August 15, 1998
Revision 2.0 (02.11.1999)

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# 1.0 INTRODUCTION

The Niagara NT 944 system board is a high reliability design for the Intel MMX and non-MMX processors, supporting speed ranges from 75-233MHz. AMD and Cyrix are supported as well up to 200MHz. The board provides four PCI slots, four ISA slots, a multi I/O controller for serial, parallel, floppy and dual FAST ATA/IDE (also called Enhanced) interface. It is recommended that this board be configured on setup with a CPU fan cooler on top of the CPU, due to the heat generated by the processor. To prevent potential dust contamination and subsequent failure, it is advised to clean this fan periodically.

## SPECIFICATIONS:

- The Niagara NT 944 is constructed on four layers with a split power plane to support lower and split plane voltage processors. It supports power regulation for all current processors with a linear power design to minimize heat dissipation and keep the processors cool. Ample decoupling capacitors, both ceramic and tantalum, smooth out any voltage spikes and keep the NT 944 well within specifications for nominal voltage.

- The NT 944 operates at all rated Bus/CPU speeds for Pentium class processors from 75MHz to 233MHz.

- Memory configurations of up to 256MB with 2 banks of two modules each per bank SIMM DRAM (minimum 8Mb). Automatic BIOS RAM configuration.

- 512KB of synchronous Burst/Pipelined cache soldered on the board.

- Supports 1 floppy port, 1 parallel port and 2 serial (16550 UART) ports. IrDA (InfraRed), USB (Universal Serial Bus) port, PS/2 mouse port and a DIN AT keyboard. All standard I/O ports use shrouded casings.

- AWARD BIOS, stored in EPROM flash. Battery backed setup.

The NT 944 system board is designed with the 82439HX PCI-bus based chip-set. It provides increased system integration for PCI-bus IDE interface and USB from the chip-set by way of a header, but also uses a fast multi I/O chip design for serial, floppy and parallel interface which supports ECP and EPP protocols. In addition a single IrDA port is provided.

All ISA and PCI expansion slots are made with nickel plated phosphorous bronze material. The CPU and memory sockets are made of beryllium copper. And finally, care must be taken when inserting CPU and memory modules into associated slots or expansion sockets to avoid damaging circuits on the board.

The NT 944 supports four 72-pin SIMM memory modules in two banks to make up a 64-bit memory bus. The smallest module must be 4Mb each of either parity or non-parity, or EDO architecture. To get an affective error correcting scheme using EDO memory a single chip of 8K size can be installed beside the cache tag RAM. The speed recommended on all memory is 60ns.

The NT 944 supports two PCI connectors, one enhanced (primary) and one standard, for four IDE devices and detects IDE hard disk types and size through the BIOS auto-detect utility.

Every board is pre-tested and burned-in for 24 hours.

# 2.0 UNPACKING

CAUTION, unless the following precautions are followed, the manufacturer cannot be held responsible for any resulting damages. The motherboard contains static-sensitive devices that can be damaged or destroyed by rough or improper handling. Use caution when touching the card, handle by the edges only. Do not touch connectors or chips. Do not remove the board from the protective bag unless you are wearing a wrist strap designed for static discharge and connected to ground.

Proceed with the following steps:

- Examine the cardboard container for any signs of external damage.
- Open the cardboard container.
- Cut the seal of the protective bag.
- Remove the board from the bag.
- Place the bag on a flat surface and the board on top.
- Examine the board for signs of damage.
- If necessary, fill out a damage report and forward copies to your supplier indicating shipping particulars.

Note: Hold the board by edges only, since there are sharp pins which could cause injury to your fingers and hands.

Do not flex or bend the board in any manner, as this may damage the PCB traces and/or surface mount component solder joints.

# 3.0 INSTALLATION

## 3.1 SYSTEM DEFAULT SETTINGS

| | |
|---|---|
| CPU Clock | 233 MHz |
| | |
| Cache RAM | Synchronous 512KB |
| Multi I/O Controller | Enabled |
| Printer ECP Mode | DMA 3 |
| Printer port, LPT1 | IRQ 7 |
| Serial COM 1 | IRQ 4 |
| Serial COM 2 | IRQ 3 |
| PS/2 Mouse | IRQ 12 |
| IDE Channel 1 | IRQ 14 |
| IDE Channel 2 | IRQ 15 |

## 3.2 QUICK INSTALLATION

Step 1
LOCATE PIN 1 ON THE CABLES YOU ARE GOING TO USE.
When attaching the internal bus cables to the on-board host adapters and the peripherals, make sure that pin 1 is maintained throughout the bus. Pin 1 is denoted on most grey ribbon cables by a red stripe. On the Niagara NT 944 system board pin 1, on all headers, is located towards the keyboard connector in the rear of the board. Check your peripheral's manual for the correct pin 1 orientation.

Step 2
CONNECT ONE END OF THE CABLE TO THE INTERNAL HEADERS.
Line up pin 1 on the cables to pin 1 on the internal header connectors for all peripheral connections to be made. Firmly, but in a straight forward fashion, as to avoid bending the pins of the internal connector, put the cable end on to the connectors, lining up pin 1 associations.

Step 3
ATTACH FREE END OF CABLE TO THE DEVICES.
If tangled, untangle the cables so they will lie freely within the cabinet when the system case cover is replaced. Install the disks or other devices as specified in the manufacturer's directions. Make sure the pin 1 orientation is maintained.

Step 4
INSERT CPU.
Make sure to maintain orientation of pin 1 for the CPU to the socket. Carefully lift the handle of the "ZIF" socket up and gently insert the Pentium chip into the socket. Press socket handle down until it locks. Set speed of CPU using switches on SW1 (See page 18 for settings). Check for and set jumpers on JP20 and JP5 to match Voltage for Intel or AMD. (See page 17 for settings)
**Note**: For CPU chips with a single voltage (eg. non-MMX) close all three jumpers from JP21.

Step 5
INSERT MEMORY
First, align each module on angle down into the keyed slot, then rotate against the centre until the metal latches lock. Please note that unlike the cables , Pin 1 is located in the direction of the CPU.

# 4.0 CONFIGURATION

**SYSTEM MEMORY CONFIGURATION**

The NT 944 supports different sizes of memory on each of the two banks. One bank (64-bit wide) is made up with 2 connectors. Different types and size cannot be mixed in one bank. Architecture supported is 1M, 2M, 4M, 8M, 16M, 64M, 128M x 36 bit with parity, or x 32-bit (without parity) as is Extended Data Out (EDO). When using EDO memory adding an 8Kb memory chip allows 1-bit ECC memory operation. No jumper is needed for any configuration. It is recommended that gold plated memory modules be used to assure error-free mating to gold memory sockets.

**CACHE MEMORY CONFIGURATION**

L2 (Level 2) cache uses 512KB of synchronous pipelined/burst cache memory which is soldered on the board.

**BIOS SETUP**

The Award BIOS provides a built-in Set-up program which allows the user to modify basic system configurations and hardware parameters. The modified data will be stored in a battery backed CMOS RAM so data will be retained when power is turned off. The information stays unchanged unless there is a configuration change in the system, such as hard drive replacement or other peripheral equipment.

**TO ENTER SETUP PROGRAM**

Power on the computer and press <DEL> key immediately, this will bring you into the BIOS CMOS SETUP UTILITY.
The menu displays all the major selection items and allows the user to select any one choice. The selection is made by moving the cursor key to the item and press <Enter>. An on-line help message is displayed at the bottom of the screen. When a selection is made the menu of selected item will appear so the user can modify selected configuration parameters.

**BIOS FEATURES SETUP**

Selecting the BIOS FEATURES SETUP option in the CMOS SETUP UTILITY menu allows the user to change system related parameters in the displayed menu. This menu shows all of the NT 944 default values as set at the factory or other installation facility. Again the user can move the cursor by pressing direction keys and <PgDn> or <PgUp> keys to exchange the parameters. This setup program provides two convenient ways to load the factory default parameters from BIOS, if shown data is corrupted. This allows the system to recover from any possible error.

**CHIP-SET FEATURES SETUP**

Choose this menu and with the <F6> key reload initial values after any hardware changes or other system changes.

**POWER MANAGEMENT SETUP**

This menu allows the user to modify power management functions of CPU and Multi I/O chip. In general these parameters should not be changed unless setup data is corrupted.

**PCI CONFIGURATION SETUP**

This program allows the user to modify PCI IRQ signals when various PCI cards are added to the PCI slots

# 5.0 CHANNELS MAP: TIME / DMA / INTERRUPT / MEMORY/ IO

## 5.1 TIME MAP

| | |
|---|---|
| Channel 0 | System timer interrupt |
| Channel 1 | DRAM refresh request |
| Channel 2 | Speaker tone generator |

## 5.2 DMA CHANNELS

| Channel | Description |
|---|---|
| 0 | Available |
| 1 | On board ECP option |
| 2 | Floppy disk |
| 3 | On board ECP (*Default) |
| 4 | Cascade for DMA controller 1 |
| 5 | Available |
| 6 | Available |
| 7 | Available |

## 5.3 INTERRUPT MAP

NMI: Parity check error

| IRQ | Description |
|---|---|
| 0 | System Timer interrupt from TIMER 0 |
| 1 | Keyboard output buffer full |
| 2 | Cascade for IRQ 8-15 |
| 3 | Serial port 2 |
| 4 | Serial port 1 |
| 5 | Parallel port 2 |
| 6 | Floppy disk drive |
| 7 | Parallel port 1 |
| 8 | RTC clock (Real Time Clock) |
| 9 | Available |
| 10 | Available |
| 11 | Available |
| 12 | PS/2 mouse |
| 13 | Math coprocessor |
| 14 | Onboard Hard disk (IDE 1) channel |
| 15 | Onboard Hard disk (IDE 2) channel |

## 5.4 MEMORY MAP

| Address Range | Size | Description |
|---|---|---|
| 00000-7FFFF | 512K | Conventional memory |
| 80000-9FBFF | 127K | Extended Conventional memory |
| 9FC00-9FFFF | 1K | Extended BIOS data area if PS/2 mouse is installed |
| A0000-C7FFF | 160K | Available for High DOS memory |
| C8000-DFFFF | 96K | Available for High DOS memory and adapter ROMs |
| E0000-EEFFF | 60K | Available for USB |
| EF000-EFFFF | 4K | Video Service Routine for Monochrome and CGA adapter |
| F0000-F7FFF | 32K | BIOS CMOS setup utility |
| F8000-FCFFF | 20K | BIOS runtime service routine (2) |
| FD000-FDFFF | 4K | Plug and Play ESCD data area |
| FE000-FFFFF | 8K | BIOS runtime service routine (1) |

## 5.5 I/O MAP

| Range | Description |
|---|---|
| 000-01F | DMA controller (Master) |
| 020-021 | Interrupt Controller (Master) |
| 022-023 | I/O ports Chip-set control registers |
| 040-05F | Timer control registers |
| 060-06F | Keyboard interface controller (8042) |
| 070-07F | RTC ports & CMOS I/O ports |
| 080-09F | DMA register |
| 0A0-0BF | Interrupt controller (Slave) |
| 0C0-0DF | DMA controller (Slave) |
| 0F0-0FF | Math coprocessor |
| 1F0-1F8 | Hard disk controller |
| 278-27F | Parallel port LPT 2 |
| 2B0-2DF | Graphics adapter controller |
| 2F8-2FF | Serial port COM 2 |
| 360-36F | Network ports |
| 378-38F | Parallel port LPT1 |
| 3B0-3BF | Monochrome & Parallel port adapter |
| 3C0-3CF | EGA adapter |
| 3D0-3DF | CGA adapter |
| 3F0-3F7 | Floppy disk controller |
| 3F8-3FF | Serial port COM1 |

# 6.0 ON BOARD PERIPHERALS

The Niagara NT 944 motherboard is using a Multi I/O chip which has power management features and supports the following controller functions: Two serial ports with NS16550 compatible UARTS, 16-bit FIFO, modem control circuitry and optional PS/2 type mouse port logic. One parallel port with multi protocol P1284 compatible interface, supporting standard and bidirectional protocol, ECP (Extended Parallel Port), ESP (Enhanced Parallel Port) with a 128-byte FIFO, capable of up to 2Mbyte/sec transfer rates. A 4Mbyte floppy disk controller using a digital data separator with data rates to 1Mbyte/seconds and support all sizes of floppies up to 2.88Myte. And finally an IDE interface for embedded drives with primary and secondary IDE address port selects

## 6.1 SERIAL PORTS

The Niagara 944 supports two built-in serial communication ports. The generic device used in this design uses a 16-bit FIFO UART and is fully register compatible with the NS16C550. The chip is driven with a clock frequency of 1.8462 MHz and supports speeds up to 56 Kbaud.

The following EIA RS-232 signals are supported:

**CTS** : This is a modem control signal. The control process can read this signal by reading bit 4 of the **(Clear to Send)**:modem status register found in the 452 chip. Bit 0 of the same register will indicate if the CTS signal has changed since the previous reading. If the interruption jumper is installed and the interrupts are enabled, each time that the CTS signal changes an interrupt is generated.

**DSR** This is a signal used by the modem to indicate that it is ready to initiate a transmission. The **(Data Set Ready)**:signal can be read by accessing bit 5 of the modem status register. Bit l of the same register indicates that the signal changed since the previous reading. The change of this signal can also, if properly configured, generate interrupts.

**DCD (Data Carrier Detect)**: When this signal is low, it indicates to the controller that a data set detected a data carrier. This signal is found in bit 7 of the modem register, and bit 3 indicates if it changed from the last reading. A change of status in this signal can produce an interrupt if properly configured.

**RNG** When low, it indicates that the modem or data set detected a telephone **(Ring Indication)**: ringing signal. The status of the signal is stored in bit 6 of the modem register. Bit 3 indicates that the signal changed since the previous reading. Like the previous signals, an interrupt is also available.

**DTR (Data Terminal Ready)**: When active (low) indicates the modem that the controller is ready to communicate. By writing to the bit 0 of the modem control register the signal can be set to low or high as required.

**RTS (Request To Send)**: If low, informs the modem that the controller is ready to send data. By programming the modem control register this signal can be set to high or low level as required.

**TX (Transmit Data)**: This signal is used to transmit the serial data from the controller to the serial device in use.

## 6. 2 PARALLEL PORT

The Niagara NT 944 system board has a single built-in bidirectional parallel port, which supports the Centronics interface

The parallel port circuitry is contained in the multi I/O device. Another application of the parallel port can be a bi-directional connection used by software to transfer files between two systems.

**PARALLEL PORT SIGNALS:**

**STROBE** - A 0.5 microsecond minimum, high, active pulse clocks data into the printer. Valid data must be present for a minimum 0.5 microseconds before and after the strobe pulse.

**AUTO FD XT** - A logical 1 causes the printer to line-feed after a line is printed.

**INIT** - A logical 0 starts the printer (50 microsecond pulse, minimum)

**SLCT IN** - A logical 1 selects the printer.

**D0-D7** - Data bus.

**ERROR** - A logical 0 means the printer has encountered an error condition.

**SLCT** - A logical 1 means the printer is selected.

**PE** - A logical 1 means the printer has selected the end of paper.

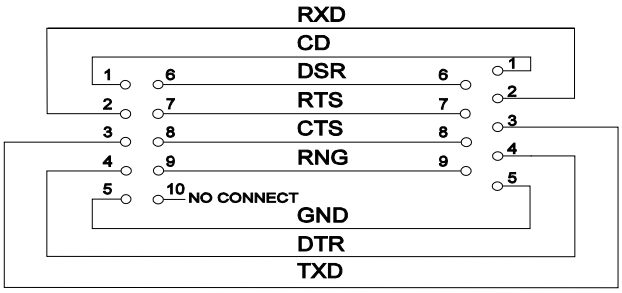
**ACK** - This line represents the current state of the printer's ACK signal. A 0 means the printer has received the character and is ready for to accept another. Normally this signal will be active for approximately 5 microseconds before BUSY stops.

**BUSY** - When this signal is active, the printer is busy and cannot accept data. It may become active during data entry, while the printer is off-line, during printing, when the printhead is changing positions or while an error state.

## 6.3 INTERNAL CABLES

### 6.3.1 SCHEMATIC DRAWING - DB9 Serial Cable

PCB Connector Female




DB9 Connector Male

NOTES:

a) PCB connector pin-out is the same as that of the header assembly on the motherboard for J12 and J13, when looking from the top. See illustration.

b) A straight forward way to make a cable requires:

- 9 wire ribbon Cable
- 10 pin (or 2 rows of 5 pins) ribbon cable insulation displacement connector (e.g. MOLEX 39-51-2104)
- DB9 flat cable insulation displacement connector (e.g. CINCH FC-09).

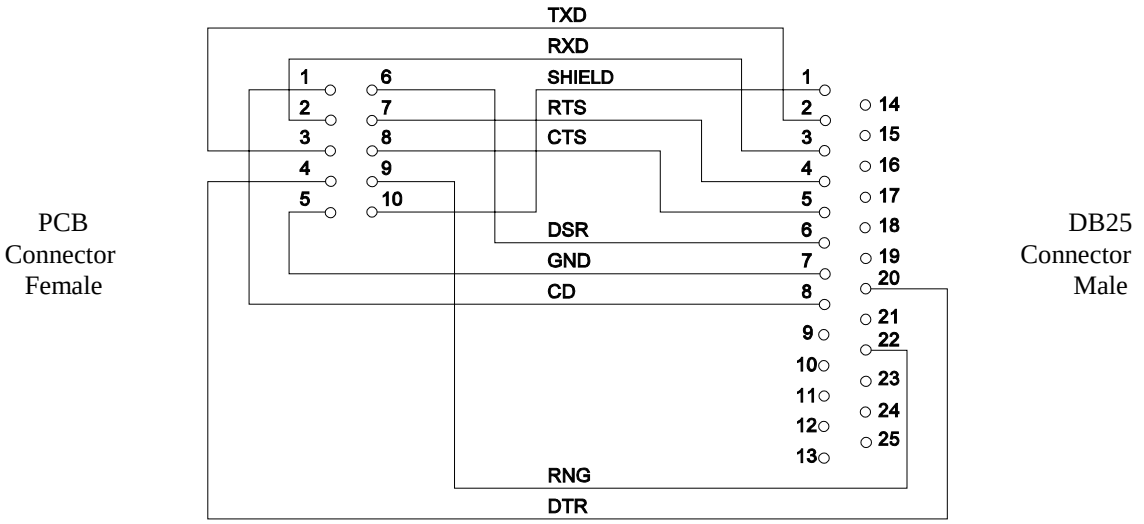
When pressing l0 pin connector, line up pin l with the red marking on the 9 wire flat cable. Similarly for the DB9 connector, line up pin l with the red marking on the flat cable.

c) The DB9 connector is IBM compatible as outlined in the document "Personal Computer AT Serial / Parallel Adapter".

d) Standard RS232 voltage level:

| | |
|---|---|
| ON : | +3V to +l5V |
| OFF : | -3V to -15V |
| INVALID: | ALL OTHERS |

### 6.3.2 SCHEMATIC DRAWING - DB25 Serial Cable




## NOTES:

a) PCB Connector pin-out is the same as that of the header assembly on the motherboard for J12 and J13 when looking from the top. See illustration.

b) PCB connector is a 10 pin (or 2 rows of 5 pins) ribbon cable insulation displacement connector
eg) MOLEX 39-51-2104

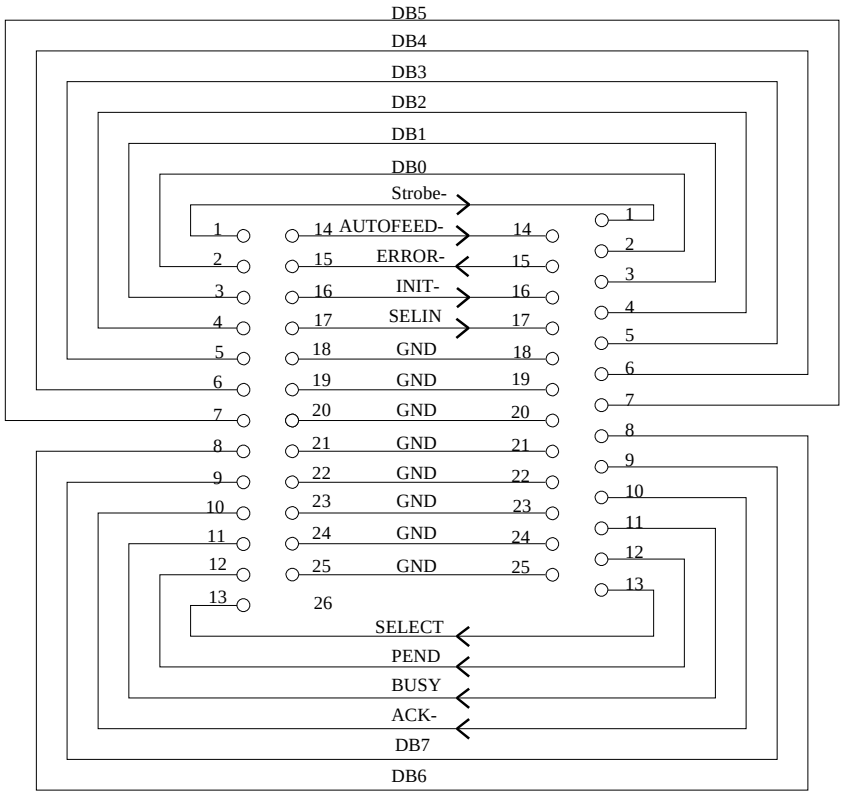
c) To make the cable requires crossing of wires in the DB 25 connector.

d) The DB 25 connector is IBM compatible as outlined in the document:
IBM Asynchronous Communication Adapter.

e) Standard RS232C voltage levels:

| | | | |
|---|---|---|---|
| ON | +3V | to | +15V |
| OFF | - 3V | to | - 15V |
| INVALID | ALL OTHERS | | |

### 9.3.3 Schematic - Parallel Cable




# NOTES:

a) PCB connector pig-out is the same as that of the header assembly on the motherboard for J9, when looking from the top.

b) A straight forward way to make a cable requires:

- 25 wire ribbon or flat cable
- 26 pin (or 2 rows of 13 pins) ribbon cable insulation displacement connector
  eg) MOLEX 39-51-2264
- DB25 flat cable insulation displacement connector
  eg) CINCH FC-25S

When pressing 26 pin connector, line up pin 1 on connector with red marking on the flat cable.

c) The DB25 connector is IBM compatible as outlined in documents:
   i) Personal Computer AT Serial/Parallel Adapter
   ii) Monochrome Display and Printer Adapter
   iii) IBM Printer Adapter

d) Standard TTL levels:

| | | | | | |
|---|---|---|---|---|---|
| DB0 - DB: | SINK CURRENT | 12 mA | ALL OTHERS: | SINK CURRENT | 2 mA |
| | SOURCE CURRENT | 2 mA | | SOURCE CURRENT | 0.2 mA |
| INIT, AUTOFEED, STROBE, SELIN: | | | ALL PINS: | HI VOLTAGE | 2.4V min |
| | SINK CURRENT | 10 mA | | LOW VOLTAGE | 0.4V max |
| | CURRENT | 0.2 mA | | | |

## 6.4 LOOPBACK PLUG: Serial Ports / Parallel Ports:

The standard connection of signals shown enables external loopback testing of such diagnostics software as:

Qaplus™ from Diagsoft
Checkit™ from Touch Stone Software

### Serial Port Loopback:

Signals:

| | | |
|---|---|---|
| RXD | ↔ | TX |
| CTS | ↔ | RTS |
| DTR | ↔ | DSR , CD, RNG |

DB9 (female) Implementation:

Connect pins 2 + 3
Connect pins 7 + 8
Connect pins 1 + 4 + 6

DB25 (female) Implementation:

Connect pins 2 + 3
Connect pins 4 + 5
Connect pins 20 + 6 + 8

### Parallel Port Loopback:

Interface Standard Centronics
Loopback Status to Commands

DB45 (male):

Connect pins 1 + 13
Connect pins 2 + 15
Connect pins 10 + 16
Connect pins 11 + 17
Connect pins 12 + 14

# APPENDIX A - BIOS

### A.1 Recoverable POST Errors

Whenever a recoverable error occurs during the power on self test (POST), the system BIOS will display an error message describing the problem in sufficient detail so it can be corrected.

Two additional recoverable errors are audible rather than displayed. The audible error generated during POST is a long tone followed by two short tones. This audible error will result form either a failing video configuration (no card installed or faulty or an invalid external ROM module that does not properly checksum to zero. Any other audible errors consisting of one long tone followed by a series of short tones will be from an external ROM module (e.g. VGA)

All codes can be displayed and output to Port 80H, and 8-bit POST diagnostic card.

### A.2 BIOS Checkpoint Codes

During POST, the BIOS signals a checkpoint by outputting a code to I/O address 80H. This code can be used to establish how far the BIOS executed through the power on sequence and what test is currently being performed. This is done to help troubleshoot faulty system boards.

If the BIOS detects a terminal error condition it will halt the POST process and attempt to display the checkpoint code on the screen. The checkpoint code written to the screen will match the code written to port 80H. The code will be written repeatedly to the screen which may cause "hash" to some CGA systems.

If the system hangs before the BIOS detects the terminal error, the value at port BOG will be the last test performed. In this case, the terminal error cannot be displayed on screen

The following is a list of checkpoint codes which are written before their respective tests.

**POST BIOS Codes**

| | |
|---|---|
| 02 | Reserved |
| 04 | Reserved |
| 03 | Initialize devices: DMA, 8259, 8254 controller, RTC chip |
| 05 | Keyboard controller test |
| 06 | Reserved |
| 07 | Verify CMOS’s R/W functionality |
| C1 | Auto-detection of on board DRAM and cache |
| C5 | Copy BIOS from ROM into E0000-FFFFF shadow RAM |
| 08 | Test the first 256K DRAM |
| 09 | Initialize cache |
| 0A | Initialize 32 interrupt vectors to handlers, Identify CPU, Initialize Power Management |
| 0B | Verify RTC, read CMOS data into BIOS stack area, assign I/O and Mem for PCI device |
| 0C | Initialize data BIOS area |
| 0D | Program chipset’s value, measure CPU speed for display and initialize, set system speed |
| 0E | Test video RAM, BIOS checksum |
| 0F | 8237 DMA controller, channel 0 test |
| 10 | DMA channel 1 test |
| 11 | DMA page register test |
| 12-13 | Reserved |
| 14 | 8254 timer 0, Counter 2 test |
| 15 | Test 8259 interrupt mask bits for channel 1 |
| 16 | Test 8259 interrupt mask bits for channel 2 |
| 17 | Reserved |
| 19 | Test 8259 functionality |
| lA - 1D | Reserved |
| 30 | Detect base memory & Extended memory size |
| 31 | Test Base memory, test Extended memory |
| 32 | Program multi I/O chip according to setup |
| 33-3B | Reserved |
| 3C | Set flag for user to enter CMOS Setup Utility |
| 3D | Initialize keyboard, install PS/2 mouse |
| 3E-3F-40 | Reserved |

| | |
|---|---|
| BF | Finalize chipset program |
| 41 | Initialize FD controller |
| 42 | Initialize HD controller |
| 43 | Initialize serial & parallel ports |
| 44 | Reserved |
| 45 | Initialize math coprocessor |
| 46-4D | Reserved |
| 4E | F1 key on errors, if any |
| 4F | Password, if needed |
| 50 | Write CMOS value in the BIOS stack area back to CMOS |
| 51 | Reserved |
| 52 | Initialize all PCI ROMs, assign IRQ, PnP (IO, IRQ, DMA), program RAM parity, |
| 61 | Turn on Level 2 cache, power management, show system configuration |
| 62 | Program NumLock, typematic rate & speed from Setup |
| 63 | Update PnP ESCD information, clear memory, boot system via INT 19H |
| FF | System boots, pass control to operating system |

All numeric entries are hexadecimal.

If error B0, Bl or 30 is detected by the BIOS, an additional word of information will be displayed to the screen and to port 80H. This word will reflect the bit or address line which failed. For example if "B0 0002" is displayed, address line 1 (represented by bit one) has failed. If "30 1020" is displayed, then data bits 12 and 5 have failed in the upper 16 bits.

The same information will be output to port 80H. The checkpoint code will be output followed by a delay, the high order byte, another delay, and then the low order byte of the error. This will be repeated continuously.

## AWARD BIOS SETUP

The Award BIOS ROM has a built-in Setup program to allow user modification of basic system configuration. This type of information is stored in battery backed RAM (Dallas chip), so that it retains the Setup information when the power is turned off. We limit the explanation of the BIOS to a minimum and recommend that the user maintains the factory setup and only change values after a thorough understanding of implications of change. In case the system has been down and lost its BIOS memory always reload the original set-up values when prompted on the respective pages of the menus or sub-menus: Load Setup Default.

NOTE: The setup-menu has been optimized for this board to meet reliability criteria of registers and timing, only after extensive tests by Niagara engineers. Unless you are a qualified engineer and understand the items function and implication of change, we recommend strongly to always re-load BIOS set-up Defaults.

**Entering Setup**

Power on the computer. After the sign-on message of the video card and "Niagara" appears, press DEL immediately after being prompted on the screen, during the POST routine (Power On Self Test).

**The Main Menu**

Once you enter Award BIOS CMOS Setup Utility, the main menu will appear on the screen. Use arrow keys to navigate though the screen. Press enter to accept or select the sub-menu.

**Standard CMOS Setup**
Here you enter, when setting the board up for a first time, Date, Time, Hard drive Selection, Floppy drives, Video

**BIOS Feature Setup**
Default values from the factory are loaded. We offer a limited choice of changes for the users' convenience. System performance will not be affected.

**Chip-set Features Setup**
In this mode the user can and should change DRAM timing to match the memory in use. Once again we recommend to retain or load factory settings by using F6: Load Bios Defaults.

**Power Management Setup**
Changes can be made to Doze Mode, Standby Mode, Suspend Mode only when it is set to "User define".

**Description of the Power Management mode selection:**

**A:** **Disabled** The system operates in normal condition (Non-Green)

**Maximum Savings** This mode will maximize the power saving capability

**Minimum Savings** This mode will minimize the power savings capability

**User Define** Allows user to define timeout parameters to control power saving time. Refer to next section B:

**B:** **HDD Standby** Timer can be set from 1-15 minutes to shut Hard drive down

**System Doze** Timer starts to count when no PM event occurs and can be set from 1 minute up to 1 hour

**System Standby** This timer stars to count when "System Doze" mode timer has timed out and no PM events occurred. Valid range is from 1 minute up to 1 hour.

**System Suspend** This function works only when the Pentium CPU is installed. The timer stars to count when "System Standby" mode timer has timed out and no "PM Events" occurred. Valid range from 1 minute up 1 hour.

**Description of the "Green Functions"**

**HDD Standby**
When system stops reading or writing to the Hard disk, the timer starts to count. The system will cut of the HDD power when timer runs off the set time. The system will not resume operation until either a read from or a write to HDD command is executed.

**Doze**
The system hardware will drop down CPU clock from normal working speed when timer timeout occurs.

**Standby**
In this mode the CPU will continue to work at slow speed. The screen will be blanked out.

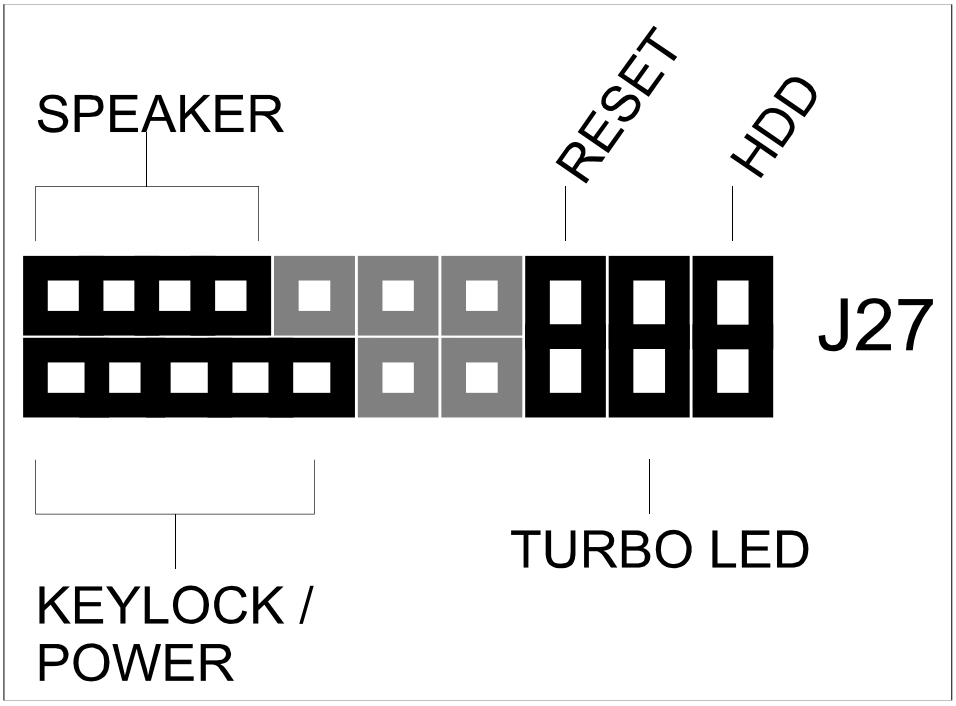
**Suspend**
When mode is timed out the chip-set will suspend the CPU clock immediately. The power consumption is even lower than in standby mode. The screen is blanked out.

**PM Events**
There are 15 PM Events in the power management mode. The user can initialize any PM Events to be "Enable" or Disable". When the system detects no activity on any of the enabled events, it will start the system "Doze" timer first. Then it will look at the "Standby" and start the countdown for it. On that timeout and other events remaining silent, the system will enter the Standby mode. By now the system will process the standby power savings procedures and start the system "Suspend" timer. Again, when this timer times out, the CPU clock will stop by dropping the system clock down to zero and will remain that way until any of the "Enable" events occur.

**PCI Configuration Setup**
When enabled the BIOS will depend on information provided by Plug and Play software (ICU) provided by the PCI card vendor in order to ensure that there are no conflicts with non PCI, (also called "Legacy") adapter cards. The ICU utility will update and save the information to the ESCD (Extend System Configuration Data).
When you have true PCI cards plugged into the system, you will not have to change anything in the SETUP program. When disabled, it is extremely important to verify the proper "Interrupt" settings to prevent system hangs.

## CONNECTORS AND JUMPER SETTINGS

| | | |
|---|---|---|
| **J30** | **12V Power connector** | For cooling fan **Please note positive (+ or red) is on right, towards CPU socket |
| **JP20** | **CPU Core Voltage** | R233: 2.8V *Default for Intel P55 (MMX)<br>R232: 3.45V<br>R231: 3.6V |
| **JP5** | **CPU I/O Voltage** | R153: 3.3V *Default for Intel P55 (MMX)<br>R156: 3.45V<br>R160: 3.6V |
| **JP1, JP4, JP21** | | Factory setting. All pins open, for MMX CPU running at 2.8V ***Default**<br>All pins closed for non-MMX CPU |
| **JP3** | **BIOS EPROM Select** | Pin 1-2 is set for 5V Flash EPROM, *Default<br>Pin 2-3 is set for 12V Flash EPROM |
| **JP2** | **Clear CMOS** | *Default = open, clears CMOS when closed |
| **J27** | **Function connectors** | Keylock / Power LED, Speaker, Turbo LED, Reset, HDD LED, |



**SW1** **CPU Clock select switch** 1=on, 0=off

Note: sw 5 was intended to switch clock circuit for non-Intel CPU clock rates. Now not implemented or supported. Leave sw 5 off at "0".

**Intel Pentium**

| | MHz | sw1 | sw2 | sw3 | sw4 | sw5 |
|---|---|---|---|---|---|---|
| | 50/75 | 1 | 1 | 0 | 0 | 0 |
| | 60/90 | 1 | 0 | 0 | 0 | 0 |
| | 66/100 | 0 | 1 | 0 | 0 | 0 |
| | 60/120 | 1 | 0 | 1 | 0 | 0 |
| | 66/133 | 0 | 1 | 1 | 0 | 0 |
| | 60/150 | 1 | 0 | 1 | 1 | 0 |
| | 66/166 | 0 | 1 | 1 | 1 | 0 |
| | 60/180 | 1 | 0 | 0 | 1 | 0 |
| | 66/200 | 0 | 1 | 0 | 1 | 0 |
| ***Default** | **66/233** | **0** | **1** | **0** | **0** | **0** |

Cyrix/IBM 6x86

| MHz | sw1 | sw2 | sw3 | sw4 | sw5 |
|---|---|---|---|---|---|
| P120+ (50/100) | 1 | 1 | 0 | 0 | 0 |
| P150+ (60/120) | 1 | 0 | 0 | 0 | 0 |
| P133+ (55/110) | call factory | | | | |
| P166+ (66/166) | call factory | | | | |

**CONNECTOR CONFIGURATIONS**

| | |
|---|---|
| **J2** | PS/2 mouse connector |
| **J26** | IrDA/IR connector |
| **J22** | USB connector |
| **J5, J6** | Serial port connectors |
| **J21** | Parallel connector |
| **J7** | Floppy disk connector |
| **IDE1** | Primary IDE connector |
| **IDE2** | Secondary IDE connector |

END